SEMESTER S8

MEMORY DESIGN AND IN-MEMORY COMPUTING

Course Code	**PEEVT 861**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	PCEVT503 VLSI Technology	**Course Type**	Elective

Course Objectives:

1. To provide an understanding of various memory types and their applications, emphasizing SRAM cell design, optimization, and the principles of memory operation in integrated circuits.

2. To enable students to design and evaluate DRAM and Flash memory systems, focusing on cell design, refresh mechanisms, memory array organization, and the intricacies of programming, erasing, and error correction.

3. To equip students with the skills to analyse timing and signal integrity in memory circuits, and to apply power optimization techniques, including power-gating and clock-gating, to enhance the efficiency of memory systems.

4. To explore in-memory computing techniques and emerging memory technologies, and to understand their applications in non-volatile storage, scientific computing, signal processing, and deep learning.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Introduction to Memory Design: Overview of memory types and their applications, Importance of memory design in integrated circuits, Basic principles of memory operation. Static Random-Access Memory (SRAM): SRAM cell design and optimization, Memory bit-cell stability and read/write operations, SRAM array architecture and peripheral circuitry.	**9**

2	Dynamic Random-Access Memory (DRAM): DRAM cell design and refresh mechanisms, Memory array organization and addressing, Timing considerations in DRAM design. Flash Memory: NAND and NOR Flash architectures, Programming and erasing mechanisms, Wear levelling and error correction in Flash memory.	**9**
3	Timing and Signal Integrity: Setup and hold time analysis, Clock-to-q delay considerations, Signal integrity challenges in memory circuits. Power Optimization in Memory Systems: Active and standby power consumption in memory, Power-gating and clock gating techniques, Low-power design strategies for memory circuits. Emerging Memory Technologies: Overview of emerging memory technologies.	**9**
4	In-memory computing: Memory devices and applications, Memory devices and computational primitives, Charge-based memory devices & Computational primitives, Resistance-based memory devices & Computational primitives, Phase change memory. Applications: Non-volatile binary storage, Scientific computing, Signal processing & Optimization, Deep learning.	**9**

Course Assessment Method
(CIE: 40 marks , ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

	Course Outcome	Bloom's Knowledge Level (KL)
CO1	Understand and design various memory types, including SRAM, by applying fundamental principles of memory operation and optimizing SRAM cell stability and array architecture.	**K2**
CO2	Design and analyse DRAM and Flash memory systems, focusing on cell design, refresh mechanisms, array organization, and addressing, as well as programming, erasing, and error correction techniques.	**K4**
CO3	Perform timing and signal integrity analysis in memory circuits and apply power optimization techniques, including power-gating and clock-gating, to enhance the efficiency of memory systems.	**K3**
CO4	Explore and implement in-memory computing techniques and emerging memory technologies, understanding their applications in non-volatile storage, scientific computing, signal processing, and deep learning.	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**2**	**1**	**1**	**1**	**2**	**1**						
CO2	**2**	**2**	**3**	**2**	**2**	**1**						
CO3	**2**	**1**	**2**	**1**	**2**	**1**						
CO4	**2**	**1**	**2**	**1**	**2**	**1**						

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	VLSI Memory Chip Design	Kiyoo Itoh	Springer	2013
2	VLSI-Design of Non-Volatile Memories.	G Campardo, R. Micheloni, D. Novosel	Springer	2005
3	Extreme Statistics in Nanoscale Memory Design	Amith Singhee, Rob A Rutenbar	Springer	2010.

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Resistive Random Access Memory (RRAM): From Devices to Array Architectures	Shimeng Yu	Springer Nature	2022
2	High-Bandwidth Memory Interface	Chulwoo Kim, Hyun-Woo Lee, Junyoung Song	Springer	2013
3	Memory Systems: Cache, DRAM, Disk	Bruce Jacob, Spencer Ng, David Wang	Morgan Kaufmann	2010

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/117/101/117101058/
2	https://www.youtube.com/watch?v=OeRk8XZnk0s
3	https://onlinecourses.nptel.ac.in/noc24_ee67/preview
4	https://www.youtube.com/watch?v=BTnr8z-ePR4